PENDING CLAIMS AS AMENDED

Please amend the claims as follows:

1. (currently amended) A CDMA demodulator, comprising:

a finger timing unit for generating signals indicating cycle boundaries for a plurality of fingers; and

an offline processing unit for receiving and storing samples and processing symbols from the stored samples for the plurality of fingers, the processing of symbols initiated in response to the cycle boundary signals.

2. (currently amended) ~~The demodulator of claim 1,~~ A CDMA demodulator, comprising:

a finger timing unit for generating signals indicating cycle boundaries for a plurality of fingers;

an offline processing unit for receiving and storing samples and processing symbols from the stored samples for the plurality of fingers in response to the cycle boundary signals; and

~~further comprising~~ a digital signal processor (DSP) for symbol demodulating and combining the processed symbols corresponding to the plurality of fingers.

3. (currently amended) ~~The demodulator of claim 1,~~ A CDMA demodulator, comprising:

a finger timing unit for generating signals indicating cycle boundaries for a plurality of fingers;

an offline processing unit for receiving and storing samples and processing symbols from the stored samples for the plurality of fingers in response to the cycle boundary signals; and

~~further comprising~~ an engine for symbol demodulating and combining high rate symbols corresponding to the plurality of fingers.

4. (currently amended) A CDMA demodulator, comprising:

a memory for storing samples according to a memory address;

a finger timing unit for producing a time reference for each of a plurality of fingers and producing a plurality of processing cycle boundary signals therefrom;

a register for storing the memory address in response to a processing cycle boundary signal; and

a sample processor for processing samples from the memory identified in accordance with the stored memory ~~address.~~ address, the sample processing initiated in response to the cycle boundary signal.

5. (currently amended) ~~The demodulator of claim 4,~~ A CDMA demodulator, comprising:

a memory for storing samples according to a memory address;

a finger timing unit for producing a time reference for each of a plurality of fingers and producing a plurality of processing cycle boundary signals therefrom;

a register for storing the memory address in response to a processing cycle boundary signal; and

a sample processor for processing samples from the memory identified in accordance with the stored memory address, wherein the location of samples in the memory for processing in the sample processor is computed by subtracting the processing cycle length from the stored memory address.

6. (original) The demodulator of claim 4, wherein the finger timing unit comprises a plurality of counters for producing the time reference for each of the plurality of fingers.

7. (currently amended) ~~The demodulator of claim 4,~~ A CDMA demodulator, comprising:

a memory for storing samples according to a memory address;

a finger timing unit for producing a time reference for each of a plurality of fingers and producing a plurality of processing cycle boundary signals therefrom, wherein the finger timing unit comprises a single counter and a plurality of masks for producing the time reference for each of the plurality of fingers;

a register for storing the memory address in response to a processing cycle boundary signal; and

a sample processor for processing samples from the memory identified in accordance with the stored memory address.

8. (original) The demodulator of claim 4, wherein the processing cycle boundary is a symbol.

9. (currently amended) ~~The demodulator of claim 4,~~ A CDMA demodulator, comprising:

a memory for storing samples according to a memory address;

a finger timing unit for producing a time reference for each of a plurality of fingers and producing a plurality of processing cycle boundary signals therefrom;

a register for storing the memory address in response to a processing cycle boundary signal; and

a sample processor for processing samples from the memory identified in accordance with the stored memory address,

wherein the sample processor comprises:

a pseudo-random noise (PN) generator for generating PN values; and

a despreader for despreading the samples with the PN values to produce despread samples.

10. (original) The demodulator of claim 9, further comprising a register for storing the time reference corresponding to and in response to a processing cycle boundary signal.

11. (original) The demodulator of claim 10, wherein the PN generator comprises a memory, loaded with the PN sequence values, which is addressed in accordance with the stored time reference.

12. (original) The demodulator of claim 11, wherein the address is computed by subtracting the processing cycle length from the stored time reference.

13. (original) The demodulator of claim 11, wherein the address is computed by adding a base station specific offset to the stored time reference and subtracting the processing cycle length from the result thereof.

14. (original) The demodulator of claim 9, wherein the sample processor further comprises:

a Walsh generator for generating Walsh chips; and

a Walsh decover for decovering the despread samples to produce decovered samples.

15. (original) The demodulator of claim 14, wherein the sample processor further comprises an accumulator for accumulating the decovered samples for one or more channels.

16. (currently amended) ~~The demodulator of claim 4,~~ A CDMA demodulator, comprising:

a memory for storing samples according to a memory address;

a finger timing unit for producing a time reference for each of a plurality of fingers and producing a plurality of processing cycle boundary signals therefrom;

a register for storing the memory address in response to a processing cycle boundary signal;

a sample processor for processing samples from the memory identified in accordance with the stored memory address; and

~~further comprising~~ an interrupt controller for arbitrating between the plurality of processing cycle boundary signals.

17. (currently amended) ~~The demodulator of claim 4,~~ A CDMA demodulator, comprising:

a memory for storing samples according to a memory address;

a finger timing unit for producing a time reference for each of a plurality of fingers and producing a plurality of processing cycle boundary signals therefrom;

a register for storing the memory address in response to a processing cycle boundary signal;

a sample processor for processing samples from the memory identified in accordance with the stored memory address; and

~~further comprising~~ a DSP for processing and combining the results of the sample processor.

18. (original) The demodulator of claim 17, further comprising a direct memory access (DMA) controller for delivering the output of the sample processor to the DSP.

19. (currently amended) A CDMA demodulator, comprising:

means for generating signals indicating cycle boundaries for a plurality of fingers;

means for receiving and storing samples; and

means for processing symbols from the stored samples for the plurality of fingers, the symbol processing initiated in response to the cycle boundary signals.

20. (currently amended) A CDMA system including a demodulator, comprising:

a finger timing unit for generating signals indicating cycle boundaries for a plurality of fingers; and

an offline processing unit for receiving and storing samples and processing symbols from the stored samples for the plurality of fingers, the processing of symbols initiated in response to the cycle boundary signals.

21. (original) A method of CDMA demodulation, comprising:

storing received I and Q samples in a memory according to a memory address;

producing a time reference for a plurality of fingers;

generating interrupts on processing cycle boundaries according to the plurality of time references; and

processing stored samples using an offline processing unit.

22. (original) The method of claim 21, further comprising:

latching the memory address upon generating an interrupt; and

accessing the stored samples for processing using an address generated from the latched memory address.

23. (original) The method of claim 21, further comprising arbitrating between simultaneous assertions of interrupts corresponding to one or more of the plurality of time references.

24. (original) The method of claim 21, further comprising symbol demodulation and combining of the results of the offline processing unit in a DSP.

25. (original) The method of claim 24, further comprising:

performing time tracking for the plurality of time references in the DSP; and

updating the plurality of time references in accordance with the time tracking.

26. (original) The method of claim 24, further comprising:

performing power control decoding in the DSP; and

modifying transmit power in accordance with the power control decoding.